Drafts
Pending
Active
- L1: (21) (((((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and
- L2: (53) ((((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and
- L3: (3) ((((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 ne
- L4: (17) (((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 ne
- L5: (2) (((((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and
- L6: (2) (((((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 n
- L7: (35) ((((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 n

Failed
Saved
- (1497) (charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3
- (182) ((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3
- (75) (((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3
- (571) (((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3
- (85) (((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3
- (4202) (charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and (volt
- (1610) ((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and (vol
- (180) (((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and (vol

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DBs: USPAT;US-PGPUB;EPO;JPO;DERWENT;IBM_TDB
Default operator: OR

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	21	(((((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and memory) and (set$4 near3 (time adj constant))) and (delay$3 with (charg$3 precharg$3 pre-charg$3))) not battery	USPAT; US-PGPU B; EPO;	2004/06/05 17:24
2	BRS	L2	53	((((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and memory) and (set$4 near3 (time adj constant))) and (delay$3 with (charg$3 precharg$3 pre-charg$3))	USPAT; US-PGPU B; EPO;	2004/06/05 17:24
3	BRS	L3	3	((((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and (set$4 near3 (time adj2 constant))) and (delay$3 with charg$3)) and (((terminat$3 stop$4 end$3) near3 (charg$3)) with (volt$3 near3 detect$3 near3 circuit))	USPAT; US-PGPU B; EPO;	2004/06/05 17:24
4	BRS	L4	17	(((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and (set$4 near3 (time adj2 constant))) and (charg$3 near3 load)	USPAT; US-PGPU B; EPO;	2004/06/05 17:24
5	BRS	L5	2	(((((charg$3 precharg$3 pre-charg$3) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and memory) and (set$4 near3 (time adj constant))) and (delay$3 with (charg$3 precharg$3 pre-charg$3))) and (((terminat$3 stop$4 end$3) near3 (charg$3 precharg$3 pre-charg$3)) with (volt$3 near3 detect$3 near3 circuit))	USPAT; US-PGPU B; EPO;	2004/06/05 17:24
6	BRS	L6	2	(((((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and memory) and (set$4 near3 (time adj2 constant))) and (delay$3 with charg$3)) and (((terminat$3 stop$4 end$3) near3 (charg$3)) with (volt$3 near3 detect$3 near3 circuit))	USPAT; US-PGPU B; EPO;	2004/06/05 17:24
7	BRS	L7	35	((((charg$3 near3 circuit) and (time adj2 constant) and delay$3 and (volt$3 near3 detect$3)) and memory) and (set$4 near3 (time adj2 constant))) and (delay$3 with charg$3)	USPAT; US-PGPU B; EPO;	2004/06/05 17:55

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